REMARKS

The April 16, 2009 Final Office Action was based on pending Claims 1–11. By this Response, Applicant is canceling Claim 9 without prejudice or disclaimer. Claims 1–8, 10 and 11 remain as previously presented. Thus, after entry of the foregoing amendments, Claims 1–8, 10 and 11 are pending and presented for further consideration. In view of the remarks set forth below, Applicant respectfully submits that Claims 1–8, 10 and 11 are in condition for allowance.

SUMMARY OF THE OBJECTIONS AND REJECTIONS

The Final Office Action objected to the drawings for not showing every feature of the invention(s) specified in the claims.

Claims 1–11 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,215,152 to Herbert ("Herbert").

OBJECTION TO THE DRAWINGS

The Final Office Action objected to the drawings as failing to comply with 37 C.F.R. § 1.83(a) as not showing every feature of the invention specified in the claims. In particular, the Final Office Action indicated that an "another metal strip" (Claim 9) was not shown in the drawings. In an effort to place this application in condition for allowance and/or reduce the number of issues on appeal, Applicant has canceled Claim 9. Thus, Applicant respectfully submits that this objection is now moot.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102(b)

The Final Office Action rejected Claims 1–8, 10 and 11 as being anticipated by Herbert. Applicant respectfully traverses this rejection, the characterization of the pending claims, and each and every implicit and/or explicit indication of Official Notice. Moreover, in view of at least the reasons set forth below, Applicant respectfully disagrees and requests reconsideration of Claims 1–8, 10 and 11.

Independent Claim 1

Focusing on independent Claim 1, in one embodiment of Applicant's invention a semiconductor device is disclosed. The device includes a semiconductor body that is provided with a field effect transistor at a surface and that includes strongly doped

source and drain zones. The device also includes a channel region extending between the source zone and the drain zone, with a gate electrode that overlaps the channel region upon perpendicular projection thereon. Moreover, the source zone, the drain zone and the gate electrode are connected at the surface to a metal source contact, a drain contact and a gate electrode contact, respectively, in the form of metal strips.

The device also includes a further metal strip positioned between the gate electrode contact and the drain contact, which further metal strip is insulated from the semiconductor body, is locally electrically connected to the source metal strip, and forms a shield between the gate electrode and the drain contact. Furthermore, the electrical connection between the further metal strip and the source contact comprises a capacitor, and the further metal strip is provided with a connecting contact for applying an external voltage to the further metal strip.

In certain embodiments, Applicant's claimed invention advantageously provides an internal capacitor (e.g., connected to the source internally) to reduce interference.

Herbert

Herbert does not disclose the semiconductor device of Claim 1. For instance, Herbert does not disclose, among other elements, an electrical connection between the further metal strip and the source contact that comprises a capacitor.

Rather, Herbert's disclosure suggests that the gate to drain feedback capacitance of any MOSFET device must be minimized in order to maximize RF gain and minimize signal distortion (see, e.g., col. 1, lines 14–16). Moreover, Herbert further recognizes that the prior art devices using Faraday shields to achieve this purpose do not completely minimize the gate-drain capacitance and cannot be applied to vertical devices (see, e.g., col. 1, lines 52–55). Accordingly, Herbert appears to teach embodiments of MOS transistors in which shield plates are used to shield the gate and drain of the transistor (see, e.g., col. 3, lines 54-56; col. 3, lines 44–45).

With particular reference to Figure 6, Herbert does not disclose, teach or suggest an electrical connection between the further metal strip and the source contact which comprises a capacitor. Rather, Figure 6 discloses a lateral DMOS structure including shield plate (48), which minimizes gate-drain capacitance, and shield metal (70), which

"further minimizes the gate-drain capacitance by shielding any capacitance between the drain metal 64' and the gate 54" (col. 3, lines 41–44; see also col. 3, lines 27–29). Assuming *arguendo* that the shield plate (48) of Herbert corresponds to the further metal strip of independent Claim 1, no part of the disclosure in Herbert suggests electrically connecting the source metal 62' and the shield plate (48) with a capacitor. Rather, Herbert makes no mention of the shield plate (48) being connected internally, but instead only mentions that it could be connected externally to a contact, which in turn could be connected to a means for applying a voltage potential (see, e.g., col. 3, lines 36–44, col. 4, lines 30–33).

With reference to Figure 7, Herbert discloses an embodiment of the invention for a vertical DMOS transistor (see, e.g., col. 3, lines 44–45), which represents an entirely different structure than the LDMOS (lateral DMOS) structure disclosed in Figure 6 (see, e.g., col. 3, lines 36–38). However, the vertical DMOS in Figure 7 does not disclose, teach or suggest an electrical connection between the further metal strip and the source contact which comprises a capacitor. It appears that any capacitance between shield plate (48) and the source metal is *de minimis* parasitic capacitance, shielding by gate (54) and minimal due to the barrier set up by the dual-layer structure of the dielectric layer and the gate oxide. Moreover, the vertical DMOS does not include a metal strip positioned between the gate electrode contact and the drain contact. Not only does the text describing the vertical DMOS in Figure 7 refer to the shield plate in this embodiment as being made of polysilicon rather than metal (see, e.g., col. 3, lines 49–53), the shield plate is not between the electrode contact and the drain contact, as Figure 7 discloses a vertical DMOS device in which the N+ drain (34) is beneath the shield plate.

Summary

Because Herbert does not disclose each and every element of Claim 1, Applicant asserts that Claim 1 is not anticipated by Herbert.

Dependent Claims 2-8, and 10-11

Claims 2–8 and 10–11 depend from independent Claim 1 and are believed to be patentably distinguished over the cited references for the reasons set forth above with respect to Claim 1 and for the additional features recited therein.

NO DISCLAIMERS OR DISAVOWALS

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain, the Examiner is cordially invited to contact the undersigned such that the issues may be promptly resolved.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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